REMARKS/ARGUMENTS

Claims 1-5 are pending. Reconsideration is respectfully requested.

1. Rejection of Claims 1-2 and 4-5 Under §112

Claims 1-2 and 4-5 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for reciting both "feature" and "reference feature". To overcome this rejection, the claims have been amended to recite just "feature".

The claims have also been amended to provide proper antecedent basis for the claim elements, and to remove repetitive language from claim 5.

2. Rejection of claims 1 and 4 Under §103(a)

Claims 1 and 4 were rejected under 35 U.S.C. 103(a) for being unpatentable over IBM Technical Disclosure Bulletin (TDB), in view of US 5,149,976 (Sipma).

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); MPEP 2143.03. The Applicants respectfully traverse this rejection, because the claim limitations are not all taught or suggested by the prior art.

Claims 1 and 4 recite, among other things, that representing, as the total video signal accumulated, the degree of overlap between the beam on portion of the scan and the higher video level portion of the feature. The Examiner acknowledges that TDB fails to teach such a method step, but that Sipma does at Col. 6, lines 11-30, and Col. 10, lines 20-45 and 53-60, and that it would have been obvious to modify TDB with the representing step. The Applicants respectfully disagree.

The Applicant respectfully submits that the cited text portions of Sipma do not teach or suggest the claimed representing step. Col. 6, lines 11-30 reads:

> *A discrete beam dwell time and blanking state are specified for each individual pixel location. Thus, the duration of the beam dwell at each location may be adjusted from pixel to pixel, and implantation may be blocked entirely for given pixels by specifying a blanked state. This control over the beam movement, together with the*

> *capability of adjusting the beam dwell time for different pixels, is particularly advantageous in developing implantation gradients. A simple case of a gradient along a single line is illustrated in FIG. 5. With this approach the spacing between successive pixels 58 is progressively diminished, so that the pixels increasingly overlap each other as the implantation proceeds from left to right. Assuming a constant dwell time for each pixel, a doping gradient will be developed from a relatively low doping level at the left end of the line to a relatively higher doping level at the right end. To produce a gradient in the opposite direction, the pixel spacings would be progressively increased from left to right.*

This text merely teaches how long, if at all, the beam dwells at the pixel location, and how the pixel location spacings can be varied to produce a doping gradient. Col. 10, lines 20-45 reads:

> *Pixel position information can be provided either directly from the CPU to the figure store, or from the CPU through the coordinate transform system to the figure store as shown in FIG. 9. X and y pixel position data is supplied from the CPU to x and y pixel position registers 140 and 142, respectively, along respective x and y data lines 144 and 146. X and y strobe signals are applied to the respective pixel position registers on lines 148 and 150, respectively. The pixel position registers 140, 142 accumulate the pixel position data and transmit them to x and y coordinate transform circuits 152 and 154, respectively. These circuits perform the requisite coordinate system reconciliation and reformatting of the pixel position data under the control of CPU 104, and supply the re-formatted x and y pixel position data to the x and y position memories 132 and 134. A memory write signal is applied along line 156 to shift the pixel position information from the coordinate transform circuitry into the figure store memories; a time delay circuit 158 provides sufficient time for the position data to propagate through the coordinate transform system before it is clocked into the figure store memories. The memory address register and address counter 138 controls the beginning of an information load into the figure store memories, and increments the memory address positions.*

This text merely discloses how to provide for pixel position information. Finally, Col. 10, lines 53-60 reads:

> *The CPU 104 also provides a set of control bits corresponding to each pixel position. The control bits are accumulated in a control register 160, and loaded into the control bit memory 136 associated with the y pixel position memory 134. In the illustration of FIG. 9, four control bits are associated with each pixel location. The first control bit A establishes whether the beam is blanked or unblanked for that particular pixel location;*

This text merely teaches how control bits are used to indicate whether the beam is blanked or unblanked for the various pixel locations.

The Applicants respectfully submit that none of these three cited passages from Sipma appear to teach, suggest, or even contemplate a representation involving a higher video level portion of the feature, let alone the degree of overlap between the beam on portion of the scan and the higher video level portion of the feature.

Therefore, it is respectfully submitted that claims 1 and 4 are not rendered obvious by TDB and Sipma, and that this rejection should be withdrawn.

3. Rejection of Claim 2 Under §103(a)

Claim 2 was rejected under 35 U.S.C. 103(a) for being unpatentable over Sipma in view of US 6,087,659 (Adler). The Applicants respectfully traverse this rejection.

Claim 2 covers a method of determining the position of a feature within a scan by, among other things, advancing an unblanked period along the scan line for succeeding scans, sampling the amplifier output at a time delay following the unblank-blank period, arranging the successive samples for giving a video profile representative of the video profile of a slow scan with a wide beam, and mathematically processing the representative video profile to yield the position of the video edge with respect to the scan. In contrast, primary reference Sipma teaches dwelling the electron beam at locations (pixels) for predetermined dwell times, instead of using more conventional line scans (see Col. 5, lines 56-65). It is respectfully submitted that Sipma fails to result in or suggest the claim elements of claim 2, and Adler fails to remedy the deficiencies of Sipma. As detailed below, the cited portions of these references do not support the conclusion that the various claim elements are met by or disclosed by Sipma and Adler.

On page 5 of the Office Action, the Examiner states that Col. 5, lines 35-45 and Col. 11, lines 31-56 of Sipma disclose the claimed advancing step (advancing the unblank-blanked period along the line by a small increment each succeeding scan). The Applicants respectfully disagree. Col. 5, lines 35-45 reads:

> *To implant an area, the FIB is scanned across the target surface in a series of parallel, adjacent scans 54. Each scan is performed at a constant speed, so that with single scans a generally constant implantation dose is produced across the entire pattern. The beam is normally oscillated back and forth along a constant x-axis, while the target is incremented in the y direction between each successive line scan to develop a two-*

> *dimensional pattern. The beam is blanked at the end of a line scan, and remains blanked until it is again permitted to reach the target at the beginning of the next line.*

This text merely teaches blanking the beam at the end of each scan line, and incrementing the target in the y direction between scan lines. Col. 11, lines 31-56 reads:

> *To create a FIB pattern, the x and y pixel positions and the control bits are first loaded into their respective registers 140, 142 and 160. A memory write signal is then provided by the pattern clock generator 126 to move the pixel position data through the coordinate transform system and into the position memories 132 and 134, and to move the control bits into the control bit memory 136. The memory write signal then increments the memory address counter 138 so that the next memory positions are available for the next pixel position data. This sequence is repeated as required for each subsequent pixel location until all of the data for a given pattern is written into the figure store memories.*
>
> *To write a pattern from the figure store, the minor field start address is loaded from the CPU into the memory address register 138. The pattern clock generator 126 increments the memory addresses, strobes the pixel position data into the DACs 168, 170, and sets the dwell time for each pixel by adjusting the time increment between successive pixel locations in accordance with the dwell time control bits. The readout of data from the position memories 132, 134 continues until the stored pattern has been written, at which time the system can switch to another figure store and immediately begin writing another pattern while the first figure store is re-loaded.*

This text merely discloses how pixel locations and dwell times are stored and used to write the intended pattern. There simply is no teaching of advancing unblanked periods along a line of the scan by small increments in each succeeding scan as recited in claim 2. In fact, incrementing unblanked periods in successive scans in the Sipma device would appear to move the pixel locations away from their intended locations, thus rendering the Sipma device inoperative for its intended purpose. Therefore, the Applicants submit the cited portions of Sipma do not teach or suggest the claimed advancing step.

The Examiner also cites Col. 7, lines 3-7, Col. 10, lines 20-45 and Col. 15, lines 12-23 of Sipma as allegedly teaching the claimed sampling step (sampling the amplifier output by an analog-to-digital converter at a time delay following the unblank-blanked period determined by the video amplifier bandwidth). The Applicants respectfully disagree. Col. 7, lines 3-7 reads:

> *A digital signal representing the selected major field is supplied over data link 74 to a major field digital-to-analog converter 76, which in turn provides an appropriate analog signal to a drive system 78 for the octopole deflector 52.*

This text discloses the use of a digital-to-analog converter, not an analog-to-digital converter. And, the digital-to-analog converter receives a signal representing the selected major field, not from an amplifier. Col. 10, lines 20-45 reads:

> *Pixel position information can be provided either directly from the CPU to the figure store, or from the CPU through the coordinate transform system to the figure store as shown in FIG. 9. X and y pixel position data is supplied from the CPU to x and y pixel position registers 140 and 142, respectively, along respective x and y data lines 144 and 146. X and y strobe signals are applied to the respective pixel position registers on lines 148 and 150, respectively. The pixel position registers 140, 142 accumulate the pixel position data and transmit them to x and y coordinate transform circuits 152 and 154, respectively. These circuits perform the requisite coordinate system reconciliation and reformatting of the pixel position data under the control of CPU 104, and supply the re-formatted x and y pixel position data to the x and y position memories 132 and 134. A memory write signal is applied along line 156 to shift the pixel position information from the coordinate transform circuitry into the figure store memories;* ***a time delay circuit 158*** *provides sufficient time for the position data to propagate through the coordinate transform system before it is clocked into the figure store memories. The memory address register and address counter 138 controls the beginning of an information load into the figure store memories, and increments the memory address positions.*

This text does disclose a time delay circuit, but it is used for providing sufficient time for the position data to propagate through the system, not for establishing a time delay for sampling an amplifier output following the unblank-blank period as recited in claim 2. Col. 15, lines 12-23 reads:

> *After amplification, the video signal is digitized by an analog-to-digital converter 250. Averaging of successive video signals either without storage, or averaging the present signal with a stored value (for example, line averaging) can be implemented. A digitized video sample is added to previous samples in an adder 252-storage register 254 loop and/or stored in a dual port random access memory (RAM) 256. Using a dual port RAM for storage of the averaged video data allows the central computer to begin using the data as soon as local averaging is complete. A control 258 slaves the memory operation to the pattern generator.*

This text does disclose an analog-to-digital converter for the video signal, but does not appear to contemplate the amplifier bandwidth, let alone a sampling time delay determined by the video amplifier bandwidth as recited in claim 2. Therefore, the Applicants submit the cited portions of Sipma do not teach or suggest the claimed sampling step.

On page 6, the Examiner states that text portions of Adler disclose the claimed arranging and processing steps of claim 2. The Applicants respectfully disagree. The cited text merely contemplates wide beam scanning and parallel imaging, not the video profile arranged and mathematically processed as recited in claim 2. And, Adler fails to remedy the deficiencies of Sipma detailed above.

It is therefore submitted that claim 2 is not rendered obvious by Sipma and Adler, and that this rejection should be withdrawn.

4. Rejection of Claim 3 Under §103(a)

Claim 3 was rejected under 35 U.S.C. 103(a) for being unpatentable over Sipma in view of US 5,345,085 (Prior). The Applicants respectfully traverse this rejection.

On page 7, the Examiner relies on Col. 11, lines 44-56 for disclosing the claimed moving step of claim 3 (incrementally moving the plurality of pixels within the raster scan toward the video contrast feature). The Applicants respectfully disagree. Col. 11, lines 44-56 reads:

> *To write a pattern from the figure store, the minor field start address is loaded from the CPU into the memory address register 138. The pattern clock generator 126 increments the memory addresses, strobes the pixel position data into the DACs 168, 170, and sets the dwell time for each pixel by adjusting the time increment between successive pixel locations in accordance with the dwell time control bits. The readout of data from the position memories 132, 134 continues until the stored pattern has been written, at which time the system can switch to another figure store and immediately begin writing another pattern while the first figure store is re-loaded.*

This text merely discloses how pixel locations and dwell times are stored, and how the system moves from one pixel location to the next pixel location, not actually moving the pixels incrementally toward the video contrast feature as recited in claim 3. The Examiner admits that Sipma fails to disclose the integrating step (integrating the signal resulting from the plurality of pixels as the plurality of pixels move towards the video contrast feature). The Applicants respectfully traverse the Examiner's conclusion that the claimed integrating step is disclosed by Prior, because the Prior reference discloses the calibration of a single pixel by integrating a signal resulting from incremental movement of the beam adjacent the pixel being calibrated

toward an axis of the grid, not integrating a signal resulting from a plurality of pixels as the plurality of pixels are moved toward the video contrast feature.

Thus, Applicants respectfully submit claim 3 is not rendered obvious by Sipma and Prior.

5. Allowed Claim

The Applicants gratefully acknowledge the indication that claim 5 would be allowable if amend to overcome the §112 rejection. Claim 5 has been so amended.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and allowance of the case is respectfully requested.

Respectfully submitted,

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